MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

EEE3196 – INTEGRATED VLSI SYSTEMS

(EE)

4 MAC 2017
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 7 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\Phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\, R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) Figure Q1(a) shows an inverter which consists of two NMOS. Assume the following parameters; $V_{TO} = 0.43$ V, $\gamma = 0.4$, $|-2\phi_F| = 0.6$ V, $V_{SB} = V_{OUT}$ when M1 is off.

(i) Calculate V_{OH} for the inverter, when M1 is off.

(ii) Calculate V_{OL} for the inverter, when $V_{IN} = V_{DD} = 2.5$ V. Transistor M2 will be velocity saturated with $V_{DSAT} = 0.38$ V.

(iii) Given $V_{IL} = 0.5$ V and $V_{IH} = 1.3$ V, calculate the noise margins; NM_L and NM_H.

(iv) Based on your answer in (iii) and your understanding in Voltage Transfer Characteristics (VTC) and switching threshold (V_M), how can you increase the noise margin and reduce the undefined region?

[5+5+4+1 marks]

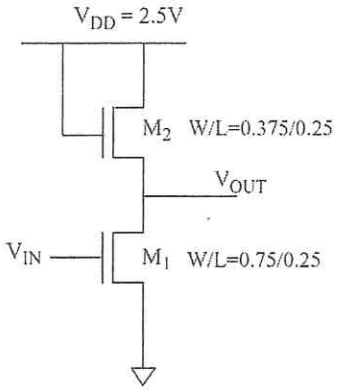

Figure Q1 (a)

(b) Given a CMOS inverter with the following parameters:
$k'_n = 115\ \mu A/V^2$, $k'_p = -30\ \mu A/V^2$, $V_{Tn} = |V_{Tp}| = 0.4$ V, $V_{DD} = 2.5$ V, $V_{GS} = 2.5$ V, (W/L)n = 0.375/0.25, (W/L)p = 1.25/0.25 and $C_L = 50$ fF.

(i) Using the average current (I_{avg}) method, find the high-to-low propagation delay (t_{PHL}).

(ii) Find the low-to-high propagation delay (t_{PLH}).

(iii) Find the total propagation delay (t_p).

[8+1+1 marks]

Continued...

Question 2

(a) Why is packaging important in the IC (Integrated Circuit) Design industry? What are the factors which could affect the right packaging?

[2+3 marks]

(b) Consider a uniform polysilicon wire with a length of 100 μm by 4 μm. It is laid parallel below an aluminium wire. The polysilicon wire is initially precharged to 2.5 V and not driven during transition. Assume that the sheet resistance of the polysilicon wire is 30 Ω/square and the capacitance of the polysilicon wire to the substrate is 50 fF. The typical interwire capacitance values are:

Area capacitance = 0.041 fF/μm^2

Fringing capacitance = 0.047 fF/μm

Assume a voltage transition at the aluminium wire from 2.5 to 0V.

(i) Calculate the total resistance of this polysilicon wire.

(ii) Calculate the total parasitic coupling capacitance associated with this line.

(iii) Calculate the voltage on the polysilicon wire, considering the voltage transition.

(iv) Propose TWO methods to reduce the capacitive crosstalk which occurs between polysilicon and aluminium wires.

[2+4+4+4 marks]

(c) Refer to Figure Q2.

(i) Describe the TWO phenomenon that happened.

(ii) Recommend ONE method to reduce the phenomenon.

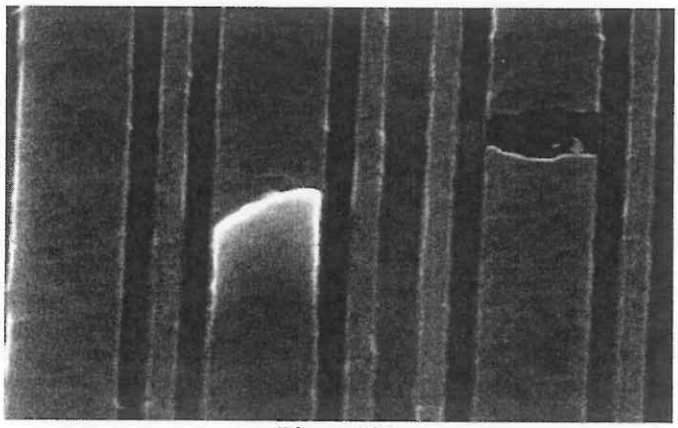

Figure Q2

[4+2 marks]

Continued...

Question 3

(a) Given the following function:

$$Y = \overline{(A + B + C).D}$$

(i) Design and sketch the circuit for this function Y using conventional static CMOS transistors.
(ii) From part (i), modify the function Y using dynamic logic.
(iii) Based on the modified design in part (ii), explain how the circuit functions.
(iv) Describe at least TWO advantages of using dynamic gates.
(v) There are also issues related to dynamic designs. Describe at least TWO issues related to dynamic gates.

[6+4+4+2+2 marks]

(b) Figure Q3 shows a circuit with alternating NMOS and PMOS logic stages. Note that the precharge-and-evaluate timing of NMOS logic stages is accomplished by the clock signal ϕ, whereas the PMOS logic stages are controlled by the inverted clock signal, $\overline{\phi}$.

(i) Describe the operation of this CMOS circuit.
(ii) State ONE advantage of this CMOS logic compared to domino CMOS logic.

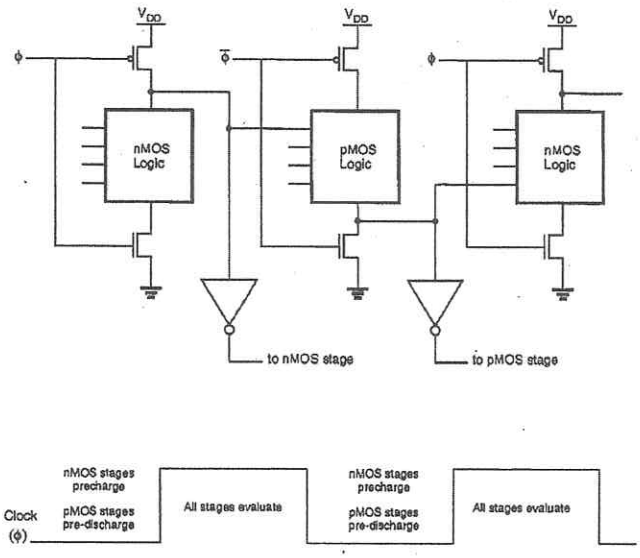

Figure Q3

[5+2 marks]

Continued...

Question 4

(a) A 1-transistor Dynamic Random Access Memory (1T DRAM) cell and the functional waveform are shown in Figure Q4(a) below.

(i) Describe the Write and Read operation of the 1T DRAM cell.
(ii) Compare the 1T DRAM with 3T (3-transistor) DRAM cell, describe TWO differences between both.

[8+4 marks]

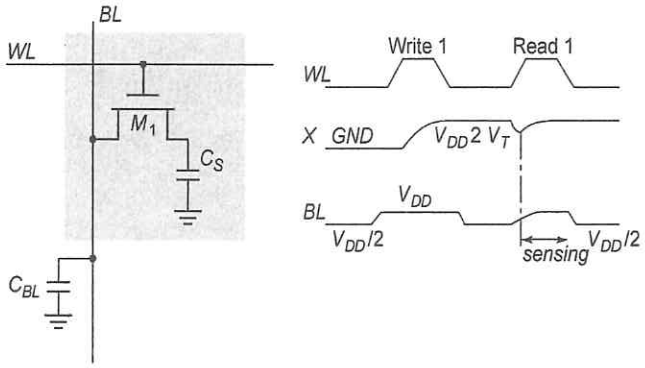

Figure Q4(a)

(b) Given a 4-bit ripple carry adder (RCA) with different delays as listed below:
$t_{carry0\rightarrow1}$ = 400 ps, $t_{carry1\rightarrow0}$ = 450 ps,
$t_{sum0\rightarrow1}$ = 500 ps, $t_{sum1\rightarrow0}$ = 550 ps.
(i) Find the worst case delay t_{adder} .
(ii) Give an example of input values that will trigger this worst case delay.

[3+2 marks]

Continued...

(c) Figure Q4(b) and Q4(c) below show graphs of area (LUT) and delay versus numbers of bit count for different types of adders respectively.
The abbreviations for these adders are:
CLA=Carry Look Ahead, RCA=Ripple Carry Adder, HW=Hard Ware, PA-BK=Brent & Kung's algorithm, CSLA=Carry Select Adder.

(i) From Figure Q4(b) and Q4(c), comment on the different adder structures which affect both the area and delay.

(ii) Based on your comment in part (i), propose the adder which serves as the generic fast parallel adder.

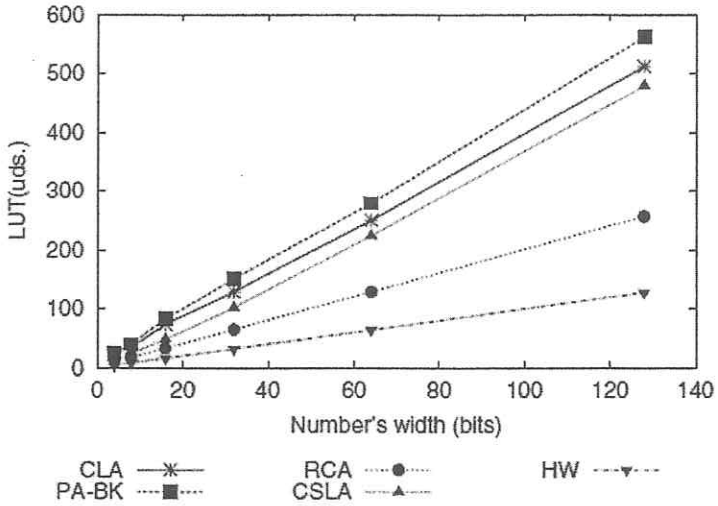

Figure Q4(b)

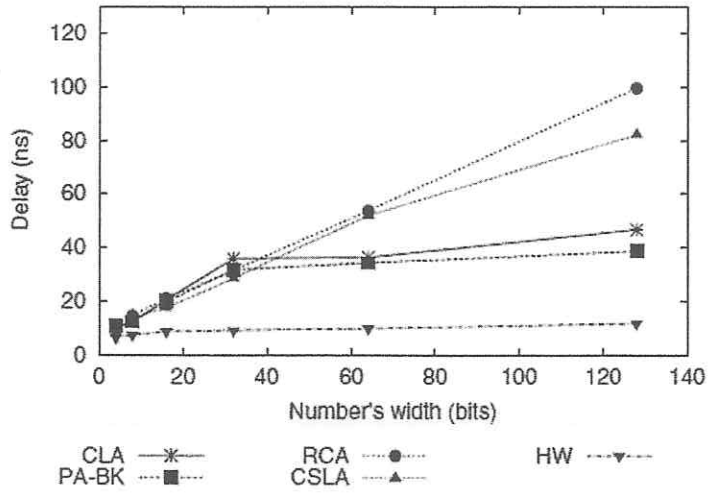

Figure Q4(c)

[6+2 marks]

End of Paper